# 18CSS201J - ANALOG AND DIGITAL ELECTRONICS

**OBSERVATION**

## Register no : Name of the student : Semester :

**Department :**





***SRM INSTITUTE OF SCIENCE AND TECHNOLOGY***

### Bharathi Salai, Ramapuram -600089

**BONAFIDE CERTIFICATE**

#### Register No

*Certified to be the bonafide record of work done by of*

*, B.Tech Degree course in the Practical* ***18CSS201J – ANALOG AND DIGITAL ELECTRONICS*** *in* ***SRM INSTITUTE OF SCIENCE***

***AND TECHNOLOGY, Ramapuram*** *during the academic year 2021-2022*

Lab In charge **HOD/ECE**

**Date:**

*Submitted for University Examination held in \_,* ***SRM INSTITUTE OF SCIENCE AND***

***TECHNOLOGY, Ramapuram.***

##### Date:

##### 

##### Examiner-1 Examiner-2

**SRM Institute of Science and Technology Department of Computer Science Engineering**

###### VISION AND MISSION OF THE DEPARTMENT

**Vision**

To become a world class department in imparting high quality knowledge and in providing students a unique learning and research experience in Computer Science and Engineering.

###### Mission

**Mission Stmt – 1** To impart knowledge in cutting edge Computer Science and Engineering technologies in par with industrial standards.

**Mission Stmt – 2** To collaborate with renowned academic institutions to uplift innovative research and development in Computer Science and Engineering and its allied fields to serve the needs of society

**Mission Stmt – 3** To demonstrate strong communication skills and possess the ability to design computing systems individually as well as part of a multidisciplinary teams.

**Mission Stmt – 4** To instill societal, safety, cultural, environmental, and ethical responsibilities in all professional activities

**Mission Stmt – 5** To produce successful Computer Science and Engineering graduates with personal and professional responsibilities and commitment to lifelong learning

###### Program Educational Objectives (PEO)

**PEO - 1** Graduates will be able to perform in technical/managerial roles ranging from design, development, problem solving to production support in software industries and R&D sectors. **PEO - 2** Graduates will be able to successfully pursue higher education in reputed institutions.

**PEO - 3** Graduates will have the ability to adapt, contribute and innovate new technologies and systems in the key domains of Computer Science and Engineering.

**PEO - 4** Graduates will be ethically and socially responsible solution providers and entrepreneurs in Computer Science and other engineering disciplines.

**PEO - 5** Graduates will possess the additional skills in core computer science discipline with knowledge of Hardware, Software , Programming , Logic & Reasoning.

###### Mission of the Department to Program Educational Objectives (PEO) Mapping

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Mission Stmt -1 | Mission Stmt -2 | Mission Stmt -3 | Mission Stmt -4 | Mission Stmt -5 |
| PEO - 1 | H | H | H | H | H |
| PEO - 2 | L | H | H | H | H |
| PEO – 3 | H | H | M | L | H |
| PEO – 4 | M | H | M | H | H |
| PEO - 5 | H | H | M | M | H |

H – High correlation, M – Medium Correlation, L – Low Correlation

###### Program Outcomes as defined by NBA (PO) Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

###### PSO – Program Specific Outcomes (PSO)

**PSO - 1** Ability to understand client requirements and suggest solutions

**PSO - 2** Ability to create Software for automation and function

**PSO - 3** Ability to utilize Logic & Reasoning Skills

Mapping Program Educational Objectives (PEO) to Program Learning Outcomes (PLO)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Program Learning Outcomes (PLO) | | | | | | | | | | | | | | |
| Graduate Attributes (GA) | | | | | | | | | | | | Program Specific Outcomes | | |
| Engineering Knowledge | Problem Analysis | Design & Development | Analysis, Design, Research | Modern Tool Usage | Society & Culture | Environment & Sustainability | Ethics | Individual & Team Work | Communication | Project Mgt. & Finance | Life Long Learning | PSO - 1 | PSO - 2 | PSO – 3 |
| PEO - 1 | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* |
| PEO - 2 | *H* | *H* | *H* | *H* | *H* | *L* | *L* | *H* | *L* | *H* | *L* | *H* | *H* | *H* | *H* |
| PEO – 3 | *H* | *H* | *H* | *H* | *H* | *L* | *L* | *L* | *L* | *L* | *H* | *H* | *H* | *H* | *H* |
| PEO – 4 | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* |
| PEO - 5 | *H* | *H* | *H* | *H* | *H* | *M* | *M* | *H* | *H* | *H* | *H* | *H* | *H* | *H* | *H* |

H – High correlation, M – Medium Correlation, L – Low Correlation

###### COURSE DESIGN

|  |  |
| --- | --- |
| **Course Learning**  **Outcomes (CLO):** | At the end of this course, learners will be able to: |
| CLO - 1 | Identify the analog and digital components in circuit design |
| CLO - 2 | Analyze the combinational and sequential logic circuits |
| CLO – 3 | Apply gates and flip-flops in circuit design |
| CLO – 4 | Use simulation package and realize |
| CLO - 5 | Apply HDL code and synthesize |
| CLO – 6 | Build the circuits in bread board and demonstrate and FGPA |

**CO PO Mapping**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Program Learning Outcomes (PLO) | | | | | | | | | | | | | | |
| Graduate Attributes (GA) | | | | | | | | | | | | Program Specific Outcomes | | |
| PO -1 | PO -2 | PO - 3 | PO - 4 | PO- 5 | PO- 6 | PO - 7 | PO- 8 | PO - 9 | PO - 10 | PO -11 | PO-12 | PSO - 1 | PSO - 2 | PSO – 3 |
| CLO - 1 | H | H | - | - | - | - | - | - | - | - | - | - | - | - | - |
| CLO - 2 | H | H | - | - | - | - | - | - | - | - | - | - | - | - | - |
| CLO – 3 | H | - | H | H |  | - | - | - | - | - | - | - | - | - | - |
| CLO – 4 | H | H | H | H | H | - | - | - | - | - | - | H | - | - | - |
| CLO - 5 | H | - | H | H | H | - | - | - | - | - | - | - | - | - | - |
| CLO – 6 | - | - | H | H | - | H | - | - | H |  | H | - | - | - | - |

###### ASSESSMENT DETAILS

CLA T1 : 5 Marks

CLA T2 : 7.5 Marks

CLA T3 : 7.5 Marks

CLA T4 : 5 Marks

###### Internal Total : 25 Marks

**External Total : 25 Marks**

**LABORATORY EXPERIMENTS MAPPED WITH CLO, PO, PSO**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Name Of the Experiments** | **CLO**  **Mapping** | **PO / PSO**  **Mapping** |
| 1 | Design and Implementation of Half Wave and Full Wave Rectifiers using simulation package and  demonstrate its working | 1 | 1,2,3,10 |
| 2 | Design and implement a Schmitt trigger using Op-Amp  using a simulation package and demonstrate its working | 1 | 1,2,3,10 |
| 3 | Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a  simulation package and demonstrate the working of it | 1 | 1,2,3,10 |
| 4 | Design and implementation of transistor as a switch | 2 | 3,10 |
| 5 | Design CMOS Inverter and measure its propagation  delay for both the rising edge and the falling edge | 2 | 1,2,10 |
| 6 | Design and implementation of Binary to gray code converters and gray to binary code conversion using logic gates.  Hardware Implementation of Code Converters Using NI  Analog Discovery | 3,6 | 1,3,5,9,10, PSO3 |
| 7 | Design and implementation of Magnitude Comparator combinational circuits using simulation package.  Hardware Implementation Using NI Analog Discovery | 3,6 | 1,3,5,9,10, PSO3 |
| 8 | Design and implementation of Synchronous sequential  circuits using Simulation Package | 4 | 1,10 |
| 9 | Implementation of SISO, SIPO, PISO and PIPO shift  registers using Flip- flops | 5 | 1,3,10,  PSO2,PSO3 |
| 10 | Design and simulation of 3-bit Synchronous up and  down counter using Multi sim | 5 | 1,3,10,  PSO2,PSO3 |
| 11 | HDL PROGRAM FOR COMBINATIONAL CIRCUITS | 5 | 1,10, PSO3 |
| 12 | HDL PROGRAM FOR Sequential Circuit CIRCUITS BINARY COUNTER | 3 | 1,3,5,9,10,  PSO3 |
| 13 | HDL PROGRAM FOR Sequential Circuit CIRCUITS MOD-10 COUNTER | 5 | 1,3,10,  PSO2,PSO3 |

**INDEX SHEET**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Exp.**  **No** | **Date of**  **Experiment** | **Name of the Experiment** | **Page**  **No** | **Marks**  **(20)** | **Staff**  **Signature** |
| 1 |  | Design and Implementation of Half Wave and Full Wave Rectifiers using simulation  package and demonstrate its working |  |  |  |
| 2 |  | Design and implement a Schmitt trigger using Op-Amp using a simulation package  and demonstrate its working |  |  |  |
| 3 |  | Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and  demonstrate the working of it |  |  |  |
| 4 |  | Design and implementation of transistor  as a switch |  |  |  |
| 5 |  | Design CMOS Inverter and measure its  propagation delay for both the rising edge and the falling edge |  |  |  |
| 6 |  | Design and implementation of Binary to gray code converters and gray to binary code conversion using logic gates.  Hardware Implementation of Code  Converters Using NI Analog Discovery |  |  |  |
| 7 |  | Design and implementation of Magnitude Comparator combinational circuits using simulation package.  Hardware Implementation Using NI  Analog Discovery |  |  |  |
| 8 |  | Design and implementation of  Synchronous sequential circuits using Simulation Package |  |  |  |
| 9 |  | Implementation of SISO, SIPO, PISO and  PIPO shift registers using Flip- flops |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 10 |  | Design and simulation of 3-bit  Synchronous up and down counter using Multi sim |  |  |  |
| 11 |  | HDL PROGRAM FOR COMBINATIONAL CIRCUITS |  |  |  |
| 12 |  | HDL PROGRAM FOR Sequential Circuit CIRCUITS BINARY COUNTER |  |  |  |
| 13 |  | HDL PROGRAM FOR Sequential Circuit CIRCUITS MOD-10 COUNTER |  |  |  |

**Total Mark :**

**Average :**

**Staff Signature :**